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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,220	05/09/2001	Shunpei Yamazaki	SEL 259	4950
7590	03/25/2004		EXAMINER	
COOK, ALEX, MCFARRON, MANZO, CUMMINGS & MEHLER, LTD. Suite 2850 200 West Adams St. Chicago, IL 60606			ABDULSELAM, ABBAS I	
			ART UNIT	PAPER NUMBER
			2674	
			DATE MAILED: 03/25/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,220	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-45 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
- 13) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
 a) The translation of the foreign language provisional application has been received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4
- 4) Interview Summary (PTO-413) Paper No(s) _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

Claim Objections

1. Claims 38 and 43 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 38 and 43 are copies of the corresponding preceding claims 37 and 42 respectively.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawasaki et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Kawasaki teaches an active matrix substrate (active matrix EL display device, col. 21, lines 43-45) comprising a pixel portion (1001) formed on a glass substrate (1000), a scan line drive circuit (1002) and a signal line drive circuit (1003). Kawasaki teaches the use of a semiconductor device comprising peripheral driver circuit, constituted by a CMOS circuit, and a pixel portion constituted by a pixel TFT on the same substrate such that N-channel type TFT formed on the pixel portion is provided with the same structure as that of the N-channel type TFT of the CMOS circuit. See col. 18, lines 3-14, col. 19, 52-54, col. 20, lines 55-60 and Fig. 9.

Regarding claim 7, in addition to what has been discussed, Kawasaki teaches a circuit diagram of EL panel (Fig. 10) including a switching TFT (84), current control TFT (86) and organic EL element (87) (col. 21, lines 36-42 & Fig. 10). Furthermore, Kawasaki teaches the use of an inverter circuit (col. 18, lines 36-37 and Fig. 7C). Kawasaki also teaches CMOS circuit (Fig. 7C) also called an inverter circuit constituting a semiconductor circuit such that inverter circuits can be combined to constitute basic logic circuitry including NAND circuit a NOR circuit or more complicated logic circuitry. See col. 18, lines 36-41.

Regarding claims 2 and 8, Kawasaki teaches the use of a plastic substrate (see col. 5, lines 65-67).

Regarding claims 3 and 9, Kawasaki teaches a formation of a pixel TFT (1010), (col. 20, lines 63-64 and Fig. 9).

Regarding claims 4 and 10, Kawasaki teaches that N-channel type TFT formed on the pixel portion is provided with the same structure as that of N-channel type TFT of the CMOS circuit (col. 19, lines 52-54).

Regarding claims 5 and 11, Kawasaki teaches an application to an active matrix EL (electro-luminescence) display device (col. 21, lines 29-31 and Fig. 10).

Regarding claims 6 and 12, Kawasaki teaches the use several electronic apparatus including a personal computer (col. 22, lines 11-22 and Fig. 11A).

Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (USPN 6107983) in view of Yamanaka et al. (USPN 6372558).

Regarding claim 13 Masuda teaches a liquid crystal display device (101) with a substrate (111), which includes driver circuits (210a, 201b, 301a, 301b), and a plurality of thin film transistors, TFTs (165) coupled with pixel electrodes (col. 5, lines 28-46 and Fig. 2). Masuda also teaches that the driving circuit (201a) includes a logic circuit section (215a), which in turn includes two 2-input NAND gates NA1 and NA2 (col. 6, lines 34-45 and Fig. 3). Furthermore, Masuda points out the use of a decoder having a plurality of logic circuits (col. 1, lines 60-67 and col. 2, lines 1-5. However, Masuda does not teach all semiconductor elements being n-channel type semiconductor elements. Yamanaka on the other hand teaches thin film transistors in the peripheral driving circuit region and the display region, which may be n-channel type.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's display system to adapt Yamanaka's use of n-channel type TFT along with a driving circuit. One would have been motivated in view of the suggestion in Yamanaka that the use of "n-channel type" TFT elements is functionally equivalent to the desired n-channel type semiconductor elements. The use of n-channel type TFT helps function a display system as taught by Yamanaka.

Regarding claim 14, Yamanaka teaches an active matrix substrate permitting structure in which the display region comprising n-channel transistors are utilized

Regarding claim 15, Yamanaka teaches the use of substrate in which a silicon material is used.

Regarding claim 16, Masuda teaches the use of TFT (165). See Fig. 2.

Regarding claim 17, Yamanaka teaches a display region constructed as electro-luminescence display.

Regarding claim 18, Yamanaka teaches an electro-optic device with respect to a display region constructed as light emitting diode display device.

Claims 19-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (USPN 6107983) in view of Yamanaka et al. (USPN 6372558) in further view of Lei (USPN 6169391).

Regarding claims 19 and 24, Masuda in view of Yamanaka has been described. In addition, Yamanaka teaches a scanning side driving circuit comprising a shift register and a buffer. Yamanaka teaches the use of shift registers (Fig. 12) that includes nMOSFT or CMOS circuit. However, Masuda does not teach first and second semiconductor elements such that a gate of the second semiconductor element is connected to a drain of the first semiconductor element. Lei on the other hand illustrates the use of transistors (Fig. 7, and Fig. 9) where a gate of transistor (51) is connected to a drain of transistor (46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's display system to incorporate Lei's arrangement of

transistors. One would have been motivated in view of the suggestion in Lei that the transistors (51, 46) as configured in Fig. 7 satisfy the desired arrangement of the two semiconductor elements. The use of transistors helps achieve a low voltage direct current for display indicators such as light emitting diodes as taught by Lei.

Regarding claims 28, 32, 36 and 41, Masuda in view of Yamanaka has been described. In addition, Yamanaka teaches a scanning side driving circuit comprising a shift register and a buffer. Yamanaka teaches the use of shift registers (Fig. 12) that includes nMOSTFT or CMOS circuit. Furthermore, Lei teaches N channel depletion mode transistor switch and N enhancement mode transistor switch. See fig. 7 and Fig. 9 respectively.

Regarding claims 20, 25, 29, 33, 37-38 and 42-43, Yamanaka teaches the use of substrate in which a silicon material is used.

Regarding claim 21, Masuda teaches the use of TFT (165). See Fig. 2

Regarding claims 22, 30 26, 34, 39 and 44, Yamanaka teaches a display region constructed as electro-luminescent display

Regarding claims 23, 27, 31, 35, 40 and 45, Yamanaka teaches an electro-optic device with respect to a display region constructed as light emitting diode display device.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts are cited for further reference.

U.S. pat. No. 6,498,596 to Nakamura et al.

U.S. Pat. No. 5,663,589 to Saitoh et al.

Art Unit: 2674

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591**. The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709**.

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is **(703) 306-0377**.

Abbas Abdulselam

Examiner

Art Unit 2674

March 11, 2004



XIAO WU
PRIMARY EXAMINER